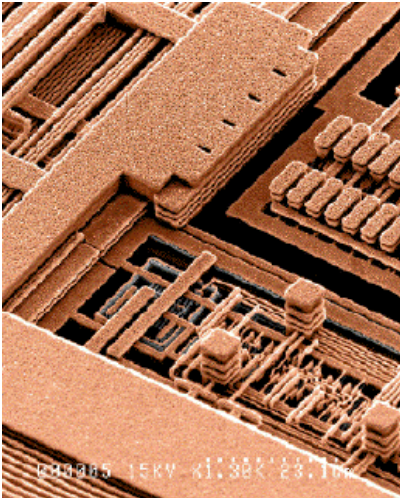


Modeling limits to conduction in nano-scale interconnects

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May 31, 2005



2003 DRAM Interconnect Roadmap Summary											
Year	Unit	2003	2004	2005	2006	2007	2008	2009	2010	2012	2015
Technology node	nm	100	90	80	70	65	57	50	45	35	25
Feature Size	nm	180	160	140	130	114	100	90	80	64	57
Resistivity	$\mu\Omega \cdot cm$	3.3	3.3	3.3	3.3	2.2	2.2	2.2	2.2	2.2	2.2

Assume no scattering (Note added in 2004 update)

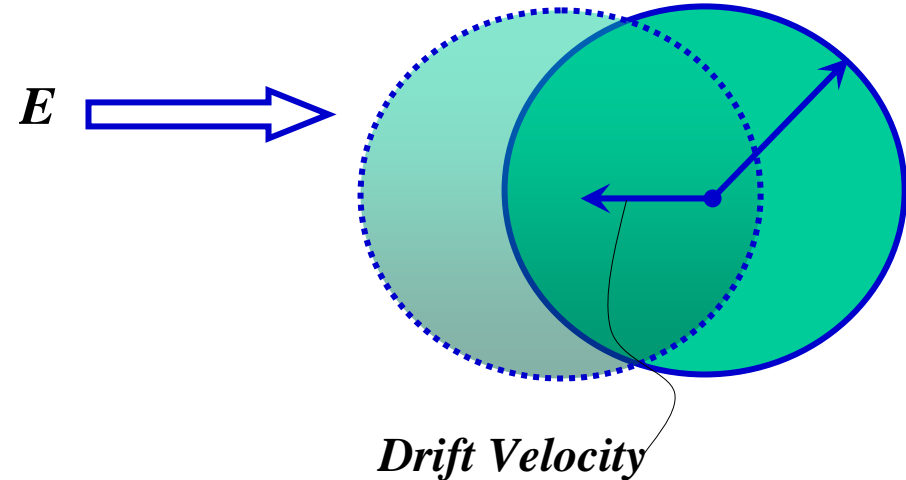
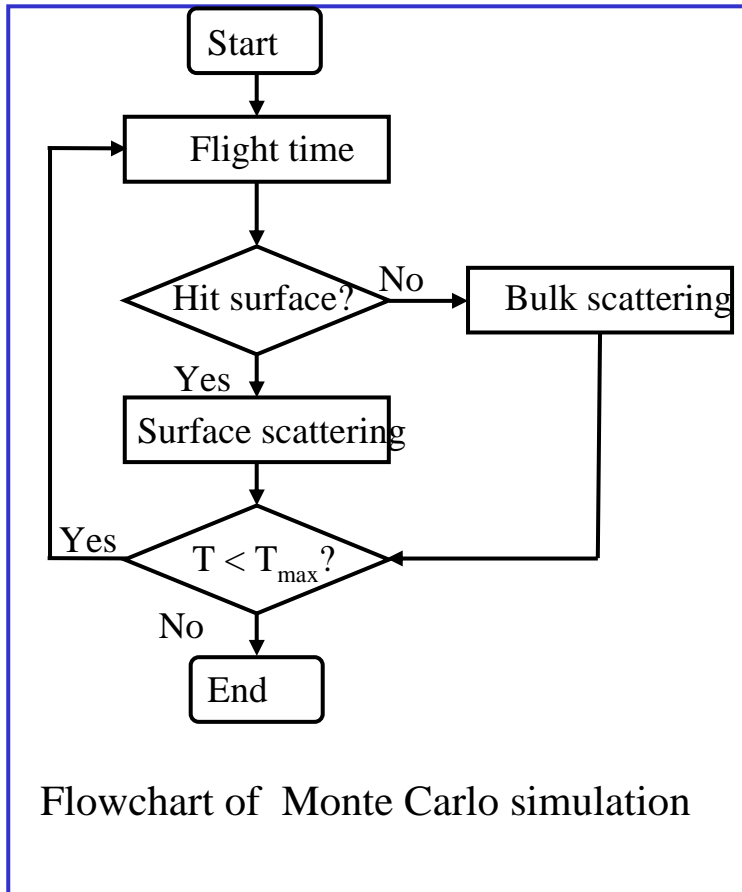
- Interconnect conductivity is an important factor for chip performance (RC delay) and power consumption
- People start to realize conductivity size effect in Nano scale interconnect



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Monte Carlo simulation of nano scale conductivity



- Electron bulk scattering is assumed as a Poisson process
- Electrons hitting on surface could be scattered diffusively or specularly, which described by a specular ratio parameter p
- $J = nev_{drift} = \sigma E$

Resistivity degradation

Resistivity Comparison of simulation and analytic forms

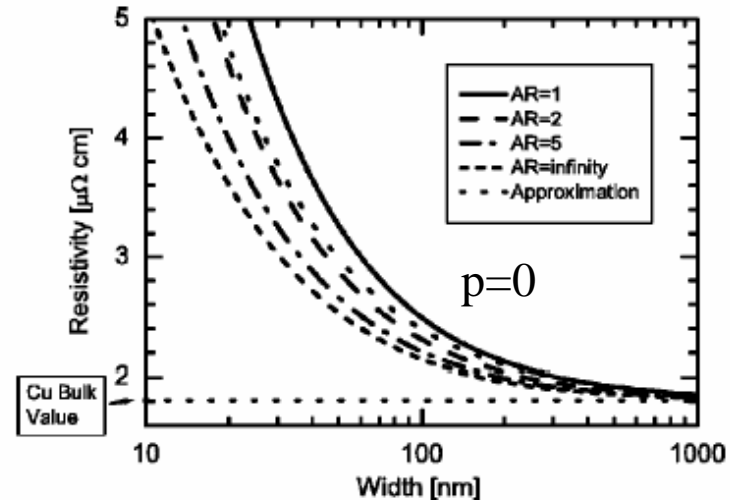
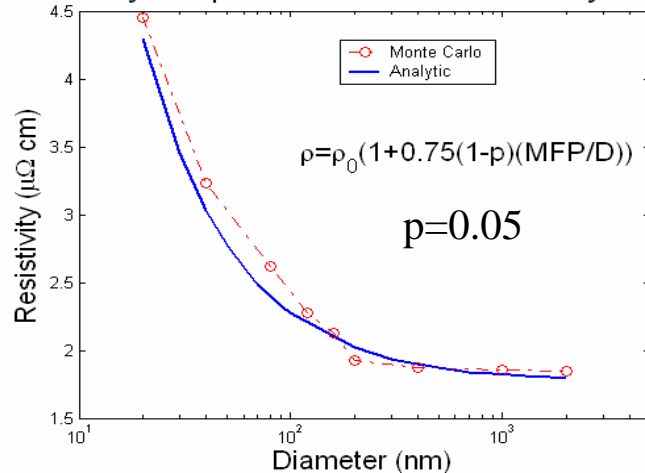


Figure and analytic form are from: W. Steinhogel, etc, PHYSICAL REVIEW B **66**, 075414 (2002)

- The idea is to incorporate surface roughness into this simulator through parameter p to see how big the contribution is.
- Beside surface roughness, grain size in polycrystalline metal wire also contribute to this resistivity size effect
- Future work will focus on decoupling these two factors with simulation.

